INTEGRATED CIRCUIT CAPACITORS
HAVING DOPED HSG ELECTRODES

Abstract of the Disclosure

Methods of forming integrated circuit capacitors include the steps of forming a lower electrode of a capacitor by forming a conductive layer pattern (e.g., silicon layer) on a semiconductor substrate and then forming a hemispherical grain (HSG) silicon surface layer of first conductivity type on the conductive layer pattern. The inclusion of a HSG silicon surface layer on an outer surface of the conductive layer pattern increases the effective surface area of the lower electrode for a given lateral dimension. The HSG silicon surface layer is also preferably sufficiently doped with first conductivity type dopants (e.g., N-type) to minimize the size of any depletion layer which may be formed in the lower electrode when the capacitor is reverse biased and thereby improve the capacitor's characteristic Cmin/Cmax ratio. A diffusion barrier layer (e.g., silicon nitride) is also formed on the lower electrode and then a dielectric layer is formed on the diffusion barrier layer. The diffusion barrier layer is preferably made of a material of sufficient thickness to prevent reaction between the dielectric layer and the lower electrode and also prevent out-diffusion of dopants from the HSG silicon surface layer to the dielectric layer. The dielectric layer is also preferably formed of a material having high dielectric strength to increase capacitance.